Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 - 2. (Canceled)

3. (Currently Amended) ~~An arrangement as claimed in claim 2, in a system including several synchronisation masters,~~ An arrangement in a communication system including a TDM bus, a number of transmitters and receivers connected to said bus, at least one synchronization master developing Frame Synchronization signals, a stable oscillator supplying a free-running data clock, and a timeslot counter in each transmitter/receiver, wherein

a free running data clock frequency is selected to give a number of periods within a frame that is always at least one more than a number of timeslots required, the periods that exceed the number of timeslots required constituting a dummy period,

wherein each timeslot counter is adapted to identify the dummy period by introducing a carry bit, which is set each time the timeslot counter exceeds the number of timeslots required; and

the frame synchronization signals are synchronized to the free-running data clock, wherein a switch over to another synchronization ~~synchronisation~~ master takes place during the dummy period if the active synchronization ~~synchronisation~~ master fails, ~~fail~~.

4 - 5. (Canceled)

6. (Currently Amended) A method ~~as claimed in claim 5~~, for synchronizing a Frame Synchronization (FS) signal and a data clock signal (CLK) in a TDM-bus system, said system including a number of transmitters and receivers connected to said bus, at least one synchronization master developing frame

synchronization signals, a stable oscillator supplying a free running data clock, and a timeslot counter in each transmitter/receiver, the method comprising the steps of:

developing the FS signal from an external communication signal;

producing the CLK signal from a stable oscillator independent of the FS signal;

selecting a frequency of said clock signal (CLK) so that a number of periods within a frame is always at least one more than the number of timeslots required, the periods exceeding this number constituting a dummy period,

wherein a carry bit is introduced in the timeslot counters to identify the dummy period, the carry bit being set each time the counters exceed the required number of timeslots on the TDM bus;

synchronizing the FS signal to the CLK signal; and

supplying the synchronized FS signal to the TDM-bus, wherein the system will switch over to another synchronization ~~synchronisation~~ master during said dummy period if [[a]] an active synchronization ~~synchronisation~~ master fails ~~fail~~